R5560/SE DAQs horizontal interconnection

Abstract

This document explains how to use the FLAG signals and fast horizontal link between DAQ.

Each DAQ is directly connected to the DAQ on the right and on the left with two kind of link:
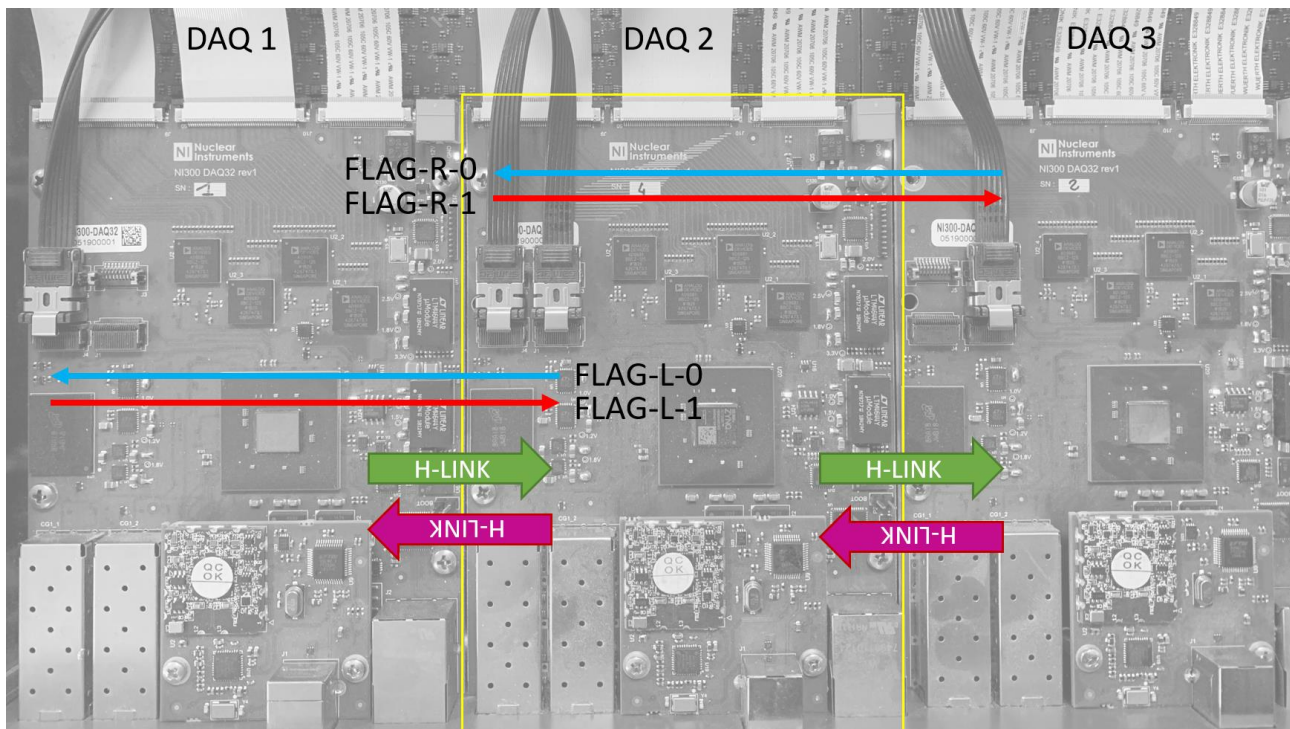
- FLAG links: two links per side (right/left), one in the direction left to right (left out, right in) the other in the opposite direction right to left (left out, right in). Flag has no propagation delay and can be used as trigger/busy/timestamp purpose
- H-LINK: two link per side (right/left), one in the direction left to right (left out, right in) the other in the opposite direction right to left (left out, right in). H-LINK is 64 bit wide and can be used to transport information between two DAQ. H-LINK has a latency of about 300ns and the latency is not deterministic.

Source code available on GitHub:

https://github.com/NuclearInstruments/r5560-daq-horizontal-interconnections

SCI-COMPILER *the configurable world*
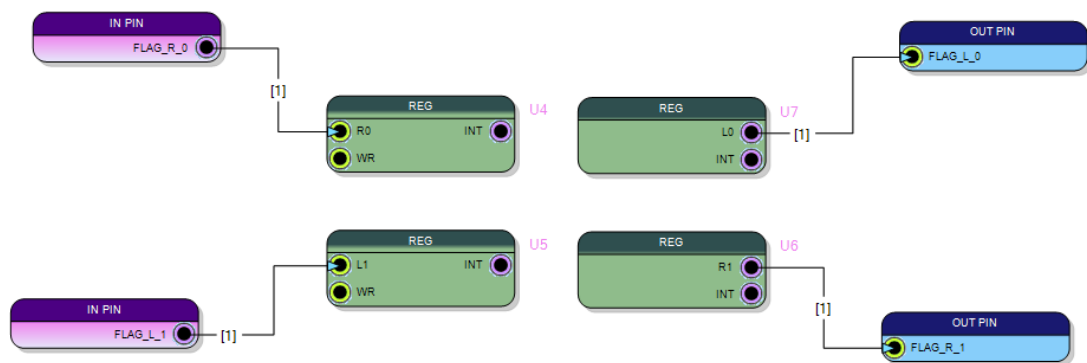
1 Interconnection on R5560/SE

The following image represents the interconnections between the DAQs inside the R5560/SE. The arrow indicates the direction of the links. The flags are single bit lines and has no latency while H-LINK are 64 bit links, operating at 125 MHz with latency of about 300 ns.
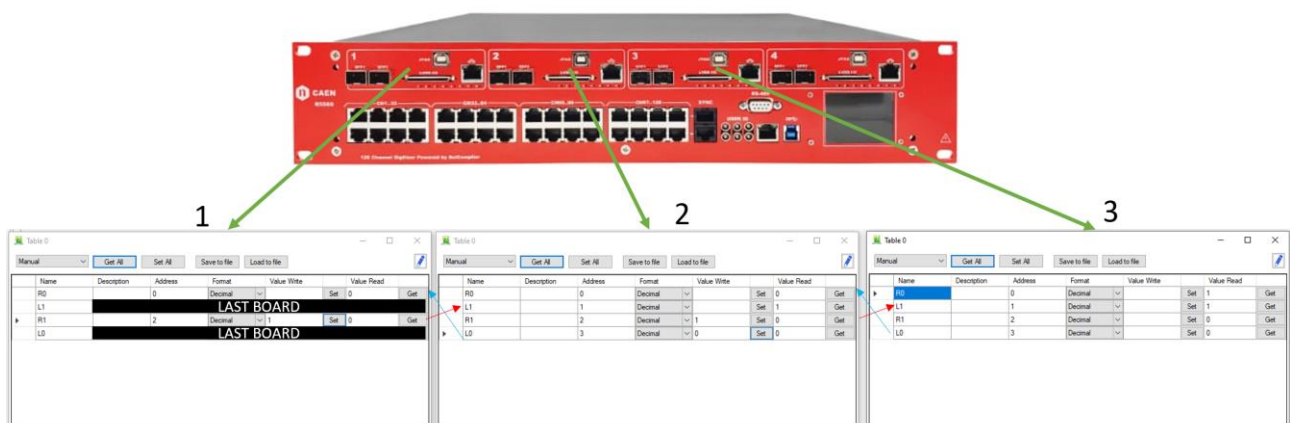

2 FLAGs lines

The flags are implemented as simply I/O with fixed direction. With reference to DAQ-2 the line has the following direction

DIRECTION (TO)	ID	BUFFER DIRECTION	CONNECTION
L	0	OUTPUT	From DAQ-2 to DAQ-1
L	1	INPUT	From DAQ-1 to DAQ-2
R	0	OUTPUT	From DAQ-2 to DAQ-3
R	1	INPUT	From DAQ-3 to DAQ-2

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The example in the repository should be loaded on all DAQ. Open multiple instances of resource explorer, on for each DAQ and connect to DAQ-1, DAQ-2, DAQ-3 (check the IP addresses on the display)

One connected, create for each DAQ a table of registers and check setting 0/1 on each output the line is commutating on the adjacent DAQ
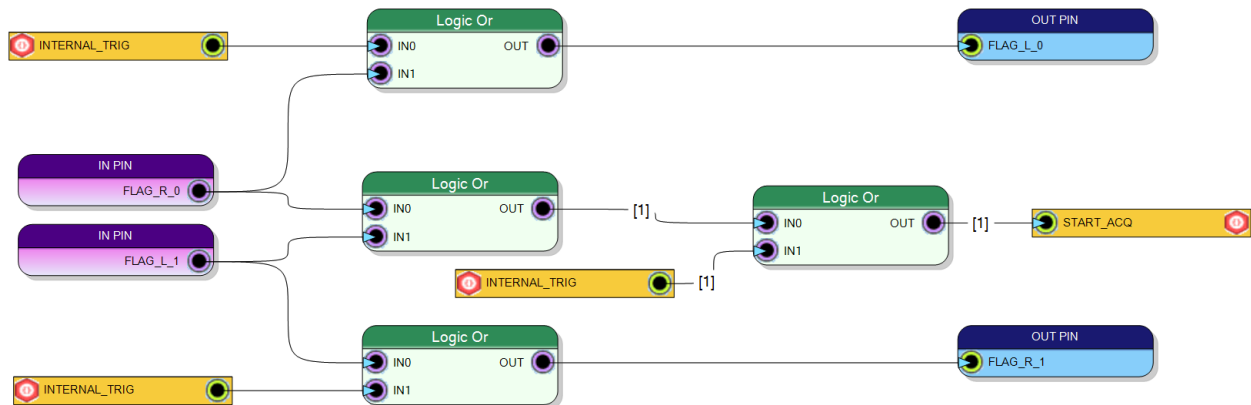

2 Use FLAGs line to implement global trigger

The flags can be used to implement an instrument level self-global trigger.

Imagine implementing a firmware where a signal called INTERNAL_TRIG in the or between all the leading-edge comparator on all 32 channels.

The internal trigger is forwarded to the DAQ on the RIGTH and on the LEFT avoiding loops: for example the DAQ 2 forward the trigger to DAQ 1 as INTERNAL_TRIGGER or DAQ3 trigger and forward the trigger to DAQ 3 as INTERNAL_TRIGGER or DAQ 1. This configuration avoid that DAQ3 or DAQ1 to trigger itself, throughout the loop inside DAQ 2. The trigger that start acquisition in DAQ2 will be the or between INTERNAL_TRIGGER, DAQ1 e DAQ3.
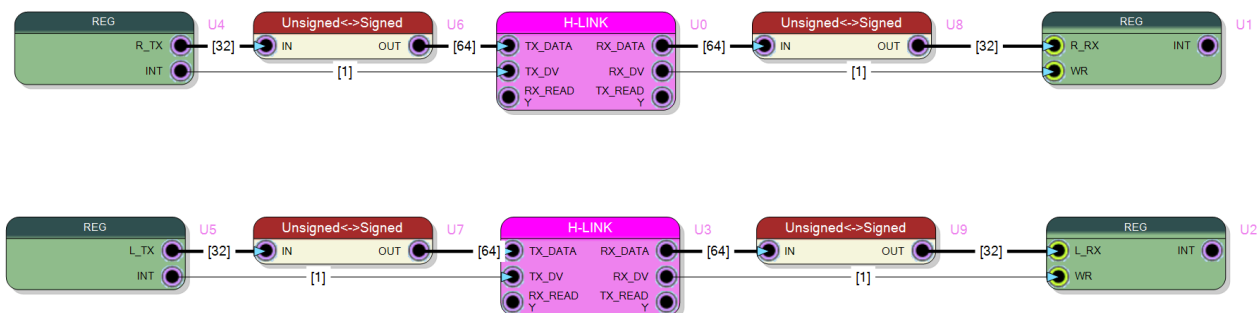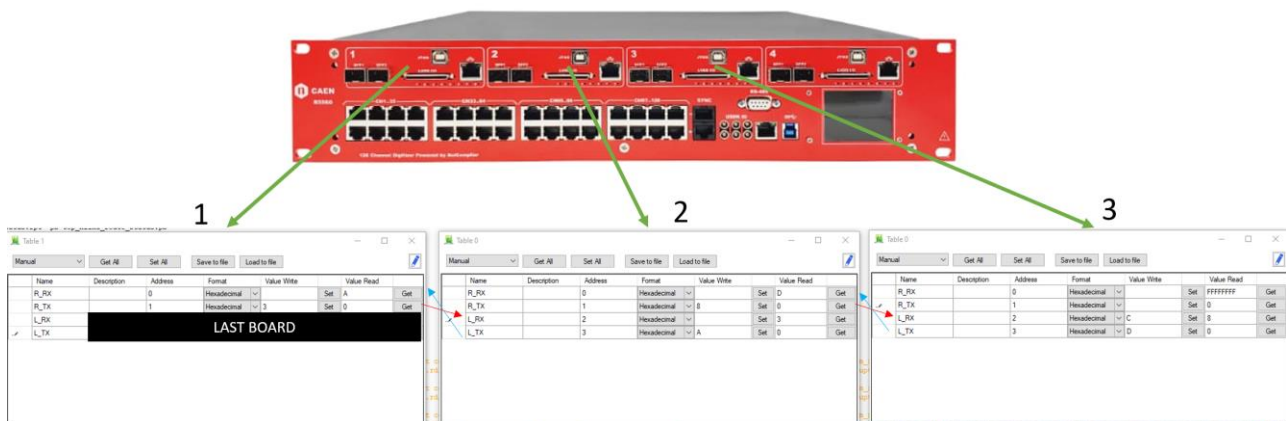
3 Use H-LINK to pass information between DAQ

The H-LINKs are bidirectional interfaces between adjacent DAQ. The HLINK uses an AURORA protocol to transport data from one DAQ to another using the 6.7 GBPS link between two FPGA.

It is important to understand that the HLINK is not a parallel bus between the FPGAs but it is as low latency serial protocol between the devices. Even if the latency is low (about 300ns), it is much more than the FLAG or a wire. More over the latency is not fixed and a jitter of tens ns can occur.

It is guaranteed that at 125 MHz it is possible to move one word of 64 bits from one DAQ to next one. The HLINK is bidirectional indeed every clock cycle a 64 bit word will be copied from DAQ 1 to DAQ 2 and 64 bits from the DAQ 2 to DAQ1. The same is true between the DAQ 2 and 3 and DAQ 3 and 4.

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4 Make deterministic H-LINK latency

If the throughput is not a problem, it is possible to make deterministic the latency of the HLINK using the FLAG signal. In this example, when a word is written to the HLINK, the flag is commutated after 500ns (delay block is set to 62 clock cycles), to be sure that the HLINK has completely transported the information on the other side. The delay on flag is fixed and grater than the latency of the HLINK; on the receiver side the delayed FLAG L->H transition samples the HLINK output make the latency deterministic. The timing of communication no more comes from the H-LINK but from the flag. H-LINK is used to carry the 64 bit information (for example which channels has been triggered on DAQ1) on the other side in order (DAQ2) to make a second level trigger logic.

Eventually the FLAG signal (which has no latency) can be used as global trigger as explained before.

TX SIDE (DAQ 1)

RX SIDE (DAQ 2)